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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,953	02/21/2007	Dietmar Birgel	BIRG3005/FJD	4797

23364 7590 08/19/2008

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EXAMINER
CHAMBERS, TRAVIS SLOAN

ART UNIT	PAPER NUMBER
2833	

MAIL DATE	DELIVERY MODE
08/19/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,953	BIRGEL ET AL.	
	Examiner	Art Unit	
	TRAVIS CHAMBERS	2833	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *response dated 06/09/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-52 and 56-58* is/are pending in the application.

4a) Of the above claim(s) *30-43 and 53-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-52 and 56-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/21/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

☐ Applicant's election without traverse of claims 44-52 and 56-58 in Papers Dated 06/09/2008 is acknowledged.

☐ Claims 30-43 and 53-55 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a non-elected invention, there being no allowable generic or linking claim.

☐ The restriction is still deemed proper and is therefore made FINAL

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 44-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Machida (4185378).

In reference to claim 44, Machida teaches a method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of: applying a foil (13a ; figure 10c) onto a surface of the circuit board (12 ; figure 10c)

following manufacture of at least one ply, or layer, of the circuit board (12) and drilling of the connection bore (14 ; figure 10c) to cover the connection bore (14); and opening (20 ; figure 10c, [Col. 7 line(s) 9-16]) the foil (13a) in the area of the connection bore (14) in such a manner that a narrowing (near lead line d ; figure 10b) in cross section of a part (end opening portion of 14) of the connection bore (14) is formed, wherein: the narrowing (near lead line d) is smaller than the wire, or pin, diameter of the electronic component and provides a holding mechanism for secure holding of the connection wire, or pin.

In reference to claim 45, Machida teaches the foil (13a) is slit in the area of the connection bore (14).

In reference to claim 46, Machida teaches the foil (13a) is provided with a hole (20) in the area of the connection bore (14).

Claim 48 is rejected under 35 U.S.C. 102(b) as being Schempp et al. (4834662).

In reference to claim 48, Schempp teaches the method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of: manufacturing a circuit board (1 ; figure 1) with at least one ply, or layer; and drilling the circuit board (1) from a surface of the circuit board (1), with a drilling tool of a nominal diameter, in such a manner that the drilling tool does not completely pass through the circuit board (1) and the connection bore (3 ; figure 1) therefore has in a region a cross section (bottom portion of 3 ; figure 1) of diameter smaller than the wire,

or pin, (distal end of 4 held in 3 ; figure 1) diameter of the electronic component, so that a narrowing brought-about thereby in the cross section of the connection bore (3) forms a holding mechanism for secure holding (in order to apply 5) of the connection wire, or pin (distal end of 4 held in 3).

Claims 49 is rejected under 35 U.S.C. 102(b) as being Reimer et al. (3670409).

In reference to claim 49, Reimer teaches the method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of: manufacturing a circuit board (12 ; figure 1) with at least one ply, or layer; completely drilling through the circuit board (12) at a location desired for the connection bore (14 ; figure 1); and placing a breaker shaped insert (18 ; figure 3) into the connection bore (14), which has a restriction (19 ; figure 3) its cross section, the diameter of the restriction (19) being smaller than the wire, or pin, (26 ; figure 7b) diameter of the electronic component, the restriction (19) representing a holding mechanism for secure holding of the connection wire, or pin (26).

Claims 50 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Belke, Jr. et al. (US 6585903 B1).

In reference to claim 50, Belke teaches a method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of:

manufacturing a circuit board (210 ; figure 12) with at least one ply, or layer; drilling a blind hole (212 ; figure 12) with a drilling tool having a desired diameter, into the circuit board (210) at a location desired for the connection bore; and drilling through the floor of the blind hole (212) with a drilling tool having a diameter smaller than the wire, or pin, diameter, in order to form a second bore (218 ; figure 12), so that a narrowing created thereby in the cross section of a part of the connection bore forms a holding mechanism (opening space created by 218 ; figure 12) for secure holding of the connection wire, or pin.

In particular reference to the recitation “for secure holding”, this is seen to be for the intended use of the claimed structure and are given little patentable weight. Further, the recitation is not seen to claim any structure that prevents the reference from being used for the same purpose as the intended use recitations of the claim.

In reference to claim 52, Belke teaches a method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of: manufacturing a circuit board (150 ; figure 9) with at least one ply, or layer; drilling a first blind hole (152 ; figure 9), at a location desired for the connection bore (154 ; figure 9), into the circuit board (150) from a first surface of the circuit board (150) with a drilling tool of a desired diameter; and drilling a second blind bore (A; image below) from a second surface (bottom surface of 150) of the circuit board (150), into the circuit board (150) a second, which is arranged essentially axially parallel and aligned with the first blind hole (152) and which meets the first blind hole (152) but does not extend

completely into it, so that, in a portion of the connection bore (154), where the two blind holes (154 and A) meet one another, a restriction is formed, which represents a holding mechanism (near lead line 156 ; figure 9) for secure holding of the connection wire, or pin.

In particular reference to the recitation “for secure holding”, this is seen to be for the intended use of the claimed structure and are given little patentable weight. Further, the recitation is not seen to claim any structure that prevents the reference from being used for the same purpose as the intended use recitations of the claim.

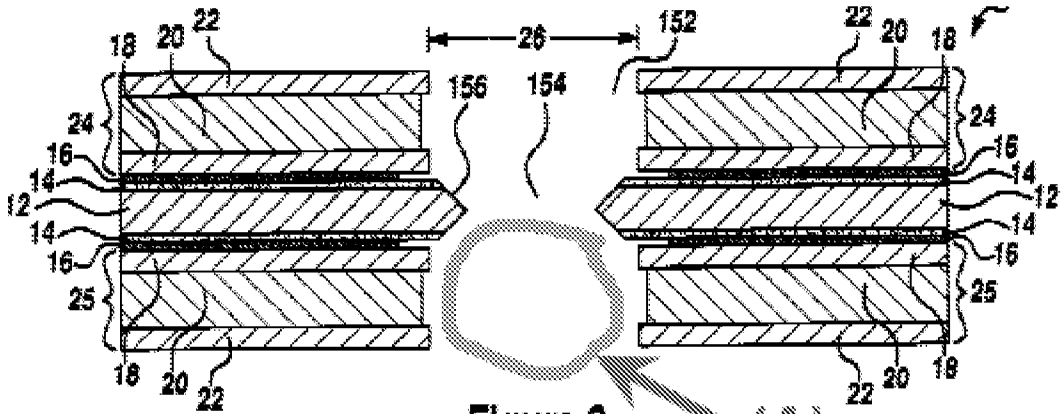

Figure 9

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (4185378) in view of Gaku et al. (US 7140103 B2).

In reference to claim 47, Machida shows substantially the invention as claimed.

However Machida does not teach the foil is opened by means of a laser.

Gaku teaches the foil is opened by means of a laser.

Therefore one of ordinary skilled in the art would have been motivated to use the teachings of Gaku because, as taught by Gaku Col. 1 line(s) 35-54, it better facilitates manufacturing by quickly sizing the hole to a satisfactory shape.

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kokubun et al. (6523257 B1) in view of Machida (4185378).

In reference to claim 51, Kokubun teaches a method for manufacturing a circuit board having at least one connection bore for receiving a connection wire, or pin, of an electronic component of a predetermined wire, or pin, diameter, comprising the steps of: manufacturing a circuit board (herein embodiment of figure 1) with at least one ply, or layer; a first blind hole (upper portion of 6; figure 1) at a location desired for the connection bore (6 ; figure 1), into the circuit board from a first surface (top surface of embodiment of figure 1) of the circuit board; and a second blind hole (bottom portion of 6 ; figure 1) from a second surface (bottom surface of embodiment of figure 1) of the circuit board, into the circuit board, which is arranged slightly offset from the first blind hole (upper portion of 6; figure 1) and which meets the first blind hole (upper portion of

6; figure 1), so that, by the offset of the two blind holes (upper and lower portion of 6 ; figure 1) relative to one another, a restriction is formed, which represents a holding mechanism for secure holding of the connection wire, or pin.

However Kokubun does not teach using a drilling tool of a desired diameter.

Machida teaches using a drilling tool (B ; figure 6a) of a desired diameter.

Therefore one of ordinary skilled in the art would have been motivated to use the teachings of Machida because it better facilitates creating a desired shaped hole by allowing better control of the depth the drill penetrates the circuit board.

In particular reference to the recitation “for secure”, this is seen to be for the intended use of the claimed structure and are given little patentable weight. Further, the recitation is not seen to claim any structure that prevents the reference from being used for the same purpose as the intended use recitations of the claim.

Claims 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (4185378) in view of Jones, Jr. et al. (4214120).

In reference to claim 56, Machida teaches populated with at lest one electronic component held in the connection bore by means of a holding mechanism.

However Machida does not teach for soldering the component in a reflow soldering oven.

Jones teaches for soldering the component (21 ; figure 6) in a reflow soldering oven (72 ; figure 7).

Therefore one of ordinary skilled in the art would have been motivated to use the teachings of Jones because it better facilitates manufacturing by allowing the electronic component to be soldered in a controlled time-temperature profile while in the oven.

In reference to claim 57, Machida teaches the component (pertaining to end portion of 15a ; figure 8) is soldered hanging beneath the circuit board (12).

However Machida does not teach of using a reflow soldering oven.

Jones teaches of using a reflow soldering oven (72 ; figure 7).

Therefore one of ordinary skilled in the art would have been motivated to use the teachings of Jones based on aesthetic/environmental requirements/preference that are driven by a desire to increase market share.

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Machida (4185378) in view of Kalina (4214353).

In reference to claim 58, Machida teaches populated with at lest one electronic component held in the connection bore by means of a holding mechanism.

However Machida does not teach soldering the component in a wave soldering facility.

Kalina teaches soldering the component in a wave soldering facility.

Therefore one of ordinary skilled in the art would have been motivated to use the teachings of Kalina because, as taught by Kalina Col. 1 line(s) 30-40, it better facilitates efficient manufacturing by allowing large-scale soldering of the components to the circuit boards in less time.

Conclusion

The prior listed on PTO form 892 that is made of record is considered pertinent to applicant's disclosure because it shows the state of the art with respect to applicant's claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRAVIS CHAMBERS whose telephone number is (571)272-6813. The examiner can normally be reached on Monday-Friday 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula Bradley can be reached on 571-272-2001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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8/14/08

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